THE AMENDED CLAIMS

The following pages provide the amended claims with the amendments marked with deleted material in [brackets] and new material underlined to show the changes made.

43. [For an electronic design automation application, a method of placing] A computer readable medium that stores a computer program that places circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a net and a plurality of circuit elements, wherein the net represents interconnections between a set of circuit elements, the [method comprising:] computer program comprising sets of instructions for:

constructing a connection graph that models the topology of interconnect lines for connecting the circuit elements of the net,

[said] wherein said connection graph having edges, each edge connecting two circuit elements of the net, wherein at least one of the edges is at least partially diagonal,

identifying a placement metric based on the connection graph.

44. The [method] computer readable medium of claim 43, wherein the set of instructions for identifying a placement metric comprises sets of instructions for: [further comprising]

calculating the length of the edges of the graph; and

combining the length calculations of the edges of the graph.

45. [The method] The computer readable medium of claim 44, wherein the set of instructions for combining of said length calculations comprises a set of instructions for adding said measurements.

46. [The method] The computer readable medium of claim 44, wherein to calculate the length of each edge that connects two circuit elements, the [method further comprises:]

computer program further comprises sets of instructions for:

a) constructing a bounding box that encompasses the two circuit elements, said bounding box having a long side with a length L and a short side with a length S, said diagonal edge forming an angle A with a side of the IC layout, wherein the two circuit elements are at two corners of the bounding box;

b) calculating the distance (D) between the two corners of the bounding box by using the equation $D= [L - \{S (\cos A / \sin A)\}] + S/\sin A$.

47. [The method] The computer readable medium of claim 46, wherein the angle A corresponds to the angle of at least one type of interconnect-line in a wiring model used by the IC layout.

48. [The method] The computer readable medium of claim 44, wherein the combined length calculation provides an estimate of interconnect-line length needed to connect the circuit elements of the net.

49. [The method] The computer readable medium of claim 48, wherein said estimate is measured to obtain a placement cost of an initial placement configuration.

50. [The method of claim 48 further comprising:] The computer readable medium of claim 48, wherein the computer program further comprises sets of instructions for:

a) modifying the position of at least one circuit elements of the net;

b) after said modification,

constructing a second connection graph that models the topology of interconnect lines for connecting the circuit elements of the net, said second graph having a number of edges, each edge connecting two circuit elements, and

calculating the length of the edges of the second connection graph,

c) to calculate the length of each edge that connects two circuit elements,

constructing a bounding box that encompasses the two circuit elements, said bounding box having a long side with a length L and a short side with a length S, wherein at least one type of interconnect-line in a wiring model used by the IC layout forms an angle A with a side of the IC layout;

calculating the length (D) of the edge by using the equation $D = [L - \{S (\cos A / \sin A)\}] + S/\sin A$.

d) combining the length calculations of the edges of the graph.

51. [The method] The computer readable medium of claim 44, wherein the IC layout includes a plurality of nets, each net having a plurality of circuit elements, [the method comprising:] wherein the computer program further comprises sets of instructions for:

a) constructing, for each particular net, [constructing] a connection graph that models the topology of interconnect lines for connecting the circuit elements of the particular net, said connection graphs having edges, wherein some of the edges are at least partially diagonal;

b) calculating the length of the edges of the graphs; and

c) combining the length calculations to obtain an estimate of the interconnect-line length needed for connecting the circuit elements of the nets.

52. [The method] The computer readable medium of claim 43, wherein the diagonal edge forms a 45° angle with respect to a side of the IC layout.

53. [The method] The computer readable medium of clam 43, wherein the diagonal edge forms a 120° angle with respect to a side of the IC layout.

54. [The method] The computer readable medium of claim 43, wherein the circuit elements include pins of circuit modules.

55. [The method] The computer readable medium of claim 43, wherein the circuit elements include circuit modules.

56. [The method] The computer readable medium of claim 43, wherein the connection graph is a minimum spanning tree.

57. [The method] The computer readable medium of claim 43, wherein the connection graph is a Steiner tree.

58. [For an electronic design automation application, a method of placing] A computer readable medium that stores a computer program that places circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a plurality of nets each of which includes a plurality of circuit elements in the IC layout, wherein the [EDA application includes] computer program uses a wiring model that defines different types of interconnect lines for connecting the circuit elements of the nets, said wiring model having diagonal lines, the [method comprising:] computer program comprising sets of instructions for:

a) defining, for each particular net, [defining] a minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net, said minimum spanning trees having edges, wherein at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal,

b) calculating the length of the edges of the minimum spanning trees; and

c) combining the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets.

59. [The method] The computer readable medium of claim 58, wherein some of the diagonal edges are in the same direction as some of the diagonal lines in the wiring model.

60. [The method of claim 58 further comprising:] The computer readable medium of claim 58, wherein the computer program further comprises sets of instructions for:

a) moving a circuit element from a first location in the IC layout to a second location in this layout;

b) defining, for each net containing the moved circuit element, [defining] a new minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net after the move, said minimum spanning trees having edges, wherein at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal,

c) calculating the length of the new minimum spanning trees to estimate the change in the total interconnect-line length.

61. [For an electronic design automation application, a method of placing] A computer readable medium that stores a computer program that places circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a plurality of nets each of which includes a plurality of circuit elements in the IC layout, wherein the [EDA application includes] computer program uses a wiring model that defines different types of interconnect lines for connecting the circuit elements of the nets, said wiring model having diagonal lines, the [method comprising:] computer program comprising sets of instructions:

a) defining, for each particular net, [defining] a Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net, said Steiner trees having edges, wherein at least one of the edges of at least one of the Steiner trees is at least partially diagonal;

b) calculating the length of the Steiner trees; and

c) combining the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets.

62. [The method] The computer readable medium of claim 61, wherein some of the diagonal edges are in the same direction as some of the diagonal lines in the wiring model.

63. [The method of claim 61 further comprising] The computer readable medium of

claim 61, wherein the computer program further comprises a set of instructions for defining a set of Steiner points for at least some of the nets.

64. The [method] computer readable medium of claim 61, wherein the computer program further [comprising] comprises sets of instructions for:

a) moving a circuit element from a first location in the IC layout to a second location in this layout;

b) for each net containing the moved circuit element, defining a new Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net after the move, said new Steiner trees having edges, wherein at least one of the edges of at least one of the new Steiner trees is at least partially diagonal,

c) calculating the length of the new Steiner trees to estimate the change in the total interconnect-line length.